IN THE CLAIMS

Please note that, pursuant to 37 CFR 1.121(c)(3), all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity and for the convenience of the Patent Office. Also attached is a version with markings to show changes made to the claims.

Please amend claims 1, 2, 5, 11, 18-25, 28, 34, 36, 41-46 as set forth below.

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1. (Twice Amended) A method for aligning a semiconductor device with a carrier substrate for electrical interconnection therebetween, the method comprising:
forming at least two channels through the semiconductor device from a first major surface thereof to a second, opposing major surface thereof;
providing a major surface of the carrier substrate with at least two alignment features spaced and positioned in respective correspondence to the at least two channels;
placing the semiconductor device over the carrier substrate; and
aligning the at least two channels formed in the semiconductor device with the at least two alignment features of the carrier substrate.

2. (Twice Amended) The method of claim 1, wherein aligning the at least two channels with the at least two alignment features includes sighting each alignment feature of the at least two alignment features through a respective corresponding channel of the at least two channels.

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3. (Previously Amended) The method of claim 1, wherein providing the major surface of the carrier substrate with at least two alignment features includes forming at least two holes in the carrier substrate.

4. The method of claim 3, wherein forming the at least two holes in the carrier substrate includes forming at least two blind holes therein.

5. (Amended) The method of claim 3, wherein aligning the at least two channels with the at least two alignment features includes placing pins through the at least two channels and into the at least two holes.

6. The method of claim 5, further comprising forming the pins of a non-conductive material.

7. The method of claim 5, further comprising forming the pins of an anti-static material.

8. The method of claim 5, further comprising affixing the pins to the semiconductor device and to the carrier substrate.

9. The method of claim 8, wherein affixing the pins to the semiconductor device and to the carrier substrate includes thermally bonding the pins to the semiconductor device and to the carrier substrate.

10. The method of claim 5, further comprising forming the pins with a mechanical self-locking mechanism proximate at least one end thereof.

11. The method of claim 5, further comprising removing the pins subsequent to the alignment of the at least two channels with the at least two alignment features.

12. (Previously Amended) The method of claim 3, wherein placing the semiconductor device over the carrier substrate is effected using a pick and place device.

13. The method of claim 12, wherein the pick and place device is used to align the semiconductor device with the carrier substrate by inserting pins carried by a head of the pick and place device through the at least two channels and the at least two holes.

14. (Previously Amended) The method of claim 13, further including lifting the pick and place device including the pins from the aligned semiconductor device and carrier substrate.

15. (Previously Amended) The method of claim 1, wherein providing the major surface of the carrier substrate with at least two alignment features includes forming at least two pins on the carrier substrate.

16. The method of claim 15, wherein forming at least two pins on the carrier substrate includes forming a mechanical locking mechanism proximate an end of each of the at least two pins.

17. (Previously Amended) The method of claim 1, wherein providing the major surface of the carrier substrate with at least two alignment features includes forming optically perceptible marks on the carrier substrate.

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18. (Amended) The method of claim 17, further comprising aligning the at least two channels with the at least two alignment features by sighting the optically perceptible marks on the carrier substrate through the at least two channels of the semiconductor device.

19. (Amended) The method of claim 18, wherein sighting the optically perceptible marks on the carrier substrate through the at least two channels includes sighting the optically perceptible marks with an optical instrument.

20. (Amended) The method of claim 1, wherein the at least two channels are each defined by a diameter and wherein the method further comprises forming at least one of the at least two channels with a larger diameter than that of at least one other channel of the at least two channels.

21. (Twice Amended) The method of claim 20, wherein providing the major surface of the carrier substrate with at least two alignment features includes correlating a size of each of

the at least two alignment features with a size of a respectively corresponding channel of the at least two channels.

22. (Amended) The method of claim 1, wherein forming the at least two channels includes forming the at least two channels in an asymmetrical pattern on the semiconductor device.

23. (Amended) The method of claim 1, wherein forming the at least two channels includes forming at least one notch on a periphery of the semiconductor device.

24. (Twice Amended) A method of testing a semiconductor device having a plurality of discrete conductive elements disposed in a pattern on a surface thereof, the method comprising:

providing a carrier substrate having a plurality of terminal pads arranged in a pattern corresponding to a mirror image of the pattern of discrete conductive elements;

forming at least two channels in the semiconductor device, each channel passing from a first surface thereof to a second, opposing surface thereof;

providing the carrier substrate with at least two alignment features, each alignment feature respectively spaced and positioned in correspondence to one of the at least two channels;

placing the semiconductor device over the carrier substrate;

aligning each channel of the at least two channels formed in the semiconductor device with a corresponding alignment feature of the at least two alignment features of the carrier substrate;

electrically contacting each discrete conductive element of the plurality with a terminal pad of the plurality; and

passing at least one electrical signal between the semiconductor device and the carrier substrate.

25. (Twice Amended) The method of claim 24, wherein aligning each of the at least two channels with a corresponding alignment feature of the at least two alignment features includes sighting each alignment feature through a corresponding channel.

26. The method of claim 24, wherein providing the carrier substrate with at least two alignment features includes forming at least two holes in the carrier substrate.

27. The method of claim 26, wherein forming at least two holes in the carrier substrate includes forming at least two blind holes.

B4 Sub. C'cont.

28. (Twice Amended) The method of claim 26, wherein aligning each of the at least two channels with a corresponding alignment feature of the at least two alignment features includes placing pins through the at least two channels and into the at least two holes.

29. (Previously Amended) The method of claim 28, further comprising forming the pins of a non-conductive material.

30. The method of claim 28, further comprising forming the pins of an anti-static material.

31. The method of claim 28, further comprising affixing the pins to the semiconductor device and to the carrier substrate.

32. The method of claim 31, wherein affixing the pins to the semiconductor device and to the carrier substrate includes thermally bonding the pins to the semiconductor device and the carrier substrate.

33. (Previously Amended) The method of claim 29, further comprising forming a mechanical self-locking mechanism proximate at least one end of each pin.

B5 Sub. C'cont

34. (Twice Amended) The method of claim 29, further comprising removing the pins subsequent to the alignment of each of the at least two channels with a corresponding alignment feature of the at least two alignment features.

35. (Previously Amended) The method of claim 27, wherein placing the semiconductor device over the carrier substrate includes using a pick and place device.

36. (Amended) The method of claim 35, wherein the pick and place device is used by placing pins carried by a head of the pick and place device through the at least two channels and the at least two holes.

37. (Previously Amended) The method of claim 36, further including lifting the pick and place device including the pins from the semiconductor device and carrier substrate.

38. The method of claim 25, wherein providing at least two alignment features in the carrier substrate includes forming pins on the carrier substrate.

39. (Previously Amended) The method of claim 38, wherein forming pins on the carrier substrate includes forming a mechanical locking mechanism proximate an end of each of the pins.

40. (Previously Amended) The method of claim 25, wherein providing at least two alignment features in the carrier substrate includes forming at least two optically perceptible marks on the carrier substrate.

41. (Amended) The method of claim 40, further comprising aligning the at least two channels with the at least two alignment features by sighting the at least two optically perceptible marks on the carrier substrate through the at least two channels of the semiconductor device.

42. (Twice Amended) The method of claim 41, wherein sighting the at least two optically perceptible marks on the carrier substrate through the at least two channels is effected using an optical instrument.

43. (Twice Amended) The method of claim 25, wherein the at least two channels are each defined by a diameter and wherein the method further comprises forming at least one of the

at least two channels with a larger diameter than that of at least one other channel of the at least two channels.

44. (Twice Amended) The method of claim 43, wherein providing at least two alignment features on the carrier substrate includes correlating a size of each alignment feature of the at least two alignment features with a size of a corresponding channel of the at least two channels.

45. (Amended) The method of claim 25, wherein forming the at least two channels includes forming the at least two channels in an asymmetrical pattern on the semiconductor device.

46. (Amended) The method of claim 25, wherein forming the at least two channels includes forming at least one notch on a periphery of the semiconductor device.